V-band MMIC LNA using Superlattice-Inserted InP Heterojunction FETs

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Millimeter-wave InP heterojunction FETs (HJFETs) with excellent low-noise performance have been developed. The HJFET features Schottky barrier layer with AlAs/InAs superlattice (SL) structure for improved thermal stability. Using the device technology, a V-band MMIC low-noise amplifier (LNA) exhibited a record noise figure (NF) of 2.0 dB at 60 GHz.

LNAs are key components in millimeter-wave systems. InP-HJFETs are attractive for these applications because of their superior noise performance at millimeter-wave frequencies compared to GaAs-based HJFETs. However, their reliability issues related to fluorine diffusion have been the main concern in applying the devices to practical systems [1]. In previous reports, we have demonstrated an InP-HJFET technology with improved thermal stability by using the SL structure in a Schottky barrier layer as well as Mo-based gate and ohmic electrodes [2][3]. However, the effect of the SL on parasitic resistance such as source resistance (Rs) has yet to be clarified since a minimum NF (NFmin) of the HJFET strongly depends on Rs. In this paper, we show that the SL-inserted HJFET is applicable to millimeter-wave MMICs with little effect on low-noise performance.

Figure 1 shows the cross section of the developed InP-HJFET. The epitaxial layers are lattice-matched to InP except for the AlAs/InAs SL layers . The SL structure serves as a diffusion barrier against fluorine atoms, which otherwise passivate Si donors in the InAlAs donor layer [1]. To further improve thermal stability, both gate and ohmic electrodes were formed using Mo.

Source resistance (Rs) of FETs is one of critical parameters which determine the noise performance. Figure 2 shows resistance network for Rs in two-layer TLM analysis. To analyze the influence of the Schottky barrier layer structure on Rs, we computed barrier resistance ρ_{12} by solving the Schrödinger equation and the Poisson equation in a self-consistent manner. It was found that the doping density (Nd) of the donor layer has much greater impact on ρ_{12} than the SL structure. We obtained the optimum Nd value of 4×10^{12} cm^{-2} by considering the trade-off between the source resistance and gate leakage current. The resulting Rs of ~0.2 Ωmm met our design goal of low-noise FETs for V-band applications.

Figure 3 shows the typical DC characteristics of the HJFET with 0.1μm-gates. The HJFET exhibited an extrinsic gm of 900 mS/mm due to low Rs with a reasonable threshold voltage of ~-0.5 V. It also showed a reasonably high gate-drain breakdown voltage of 8 V due to moderate doping of the donor layer, current gain cut-off frequency of 200 GHz and a minimum NF (NFmin) of 0.55 dB (@26 GHz).

A three-stage CPW MMIC LNA was designed and fabricated using the developed InP-HJFET. Figure 4 shows the LNA circuit. Figure 5 shows the chip photograph. The chip size is 1.1 mm × 2.5 mm. A gate width of 80 μm (40 μm × 2) was employed in order to minimize the NFmin and input matching network loss. MIM capacitors and epi-film resistors were used. The first two stages were matched for low noise. On-wafer noise measurement was carried out from 56 to 64 GHz. As shown in Fig. 6, the LNA exhibited an extremely low NF of 2.0 dB with 22.1-dB gain at 60 GHz. To the best of our knowledge, this is a record noise performance as MMIC LNAs using CPW design.

In summary, we have developed reliable InP-HJFETs with excellent low noise performance. The device technology was applied to a V-band MMIC LNA which exhibited an NF of 2.0 dB, the lowest NF ever achieved using CPW circuit at the frequency band.

REFERENCES

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[2] A. Fujihara et al., Proc. IPRM'96, part II, pp. 22-23, 1996
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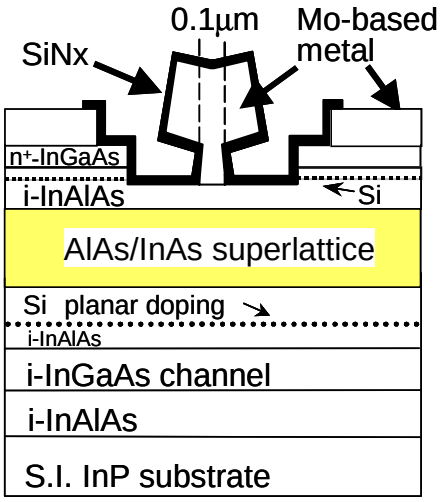

Fig. 1: Cross section of the HJFET.

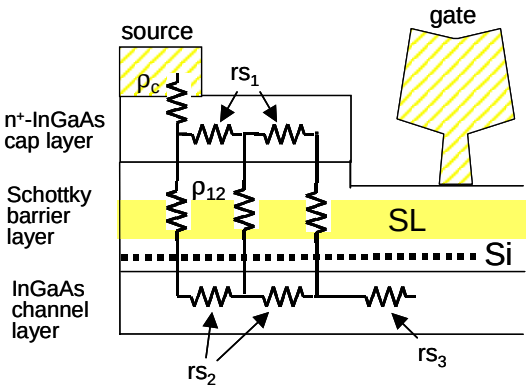

Fig. 2: Resistance network for Rs of the HJFET.

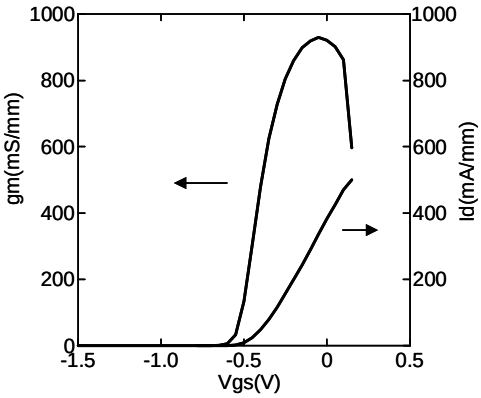

Fig. 3: Typical DC characteristics of the HJFET.

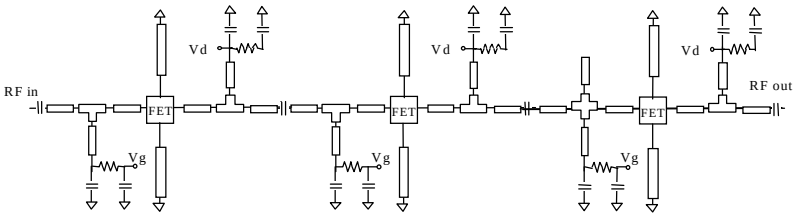

Fig. 4: The three-stage V-band LNA circuit.

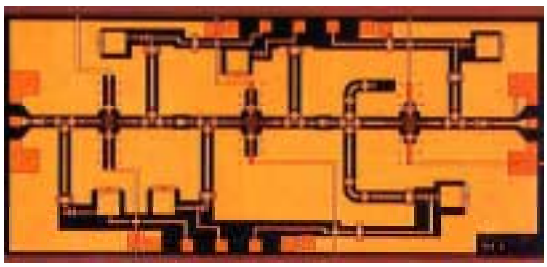

Fig. 5: Photograph of the three-stage V-band LNA.

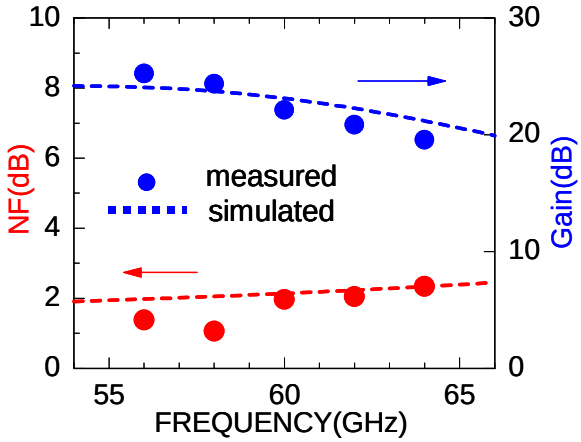

Fig. 6: Noise-performance of the LNA using the HJFETs at V-bands. Circles represent measured data. Broken lines represent simulated data.